PCN
Product/Process Change Notification

Industrial grade qualification of TVS in SMC package at Assembly/Test location in China

Notification number:	ADG-DIS/20/12014	**Issue Date**	18/02/2020
Issued by	Aline AUGIS		
Product series affected by the change		• Package: SMC • V_{BR}: 100V to 220V • Commercial Product: SM15T100A / CA to SM15T220A / CA, SMCJ85A/CA-TR to SMCJ188A/CA-TR	
Type of change		Assembly and test line transfer	

Description of the change

STMicroelectronics is qualifying according to **industrial grade** its **SMC** package subcontractor in **China**.

Reason for change

In the frame of the back-end locations management, ST has initiated a transfer of the SMC line from its Bouskoura internal plant (Morocco) to back-end partners.This **assembly** and **test plant** in China is a subcontractor already qualified and delivering in high volume for ST on automotive and industrial SMC package line.

Former versus changed product:	The changed products will remain fully compliant with product datasheet in term of electrical, dimensional and thermal parameters. Datasheet updated for SMCJ170A/CA on Ipp, Vcl and Rd parameters (10/1000µs) in coherence with SM15T200A/CA. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in packing modes and standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

As communicated in Corporate PCI 11964, ST Bouskoura SMC production line discontinuation will occur in W39-2020. Units manufactured at ST Bouskoura will be delivered till stock depletion.

Marking and traceability

Parts produced in China are differentiated by their **marking** as indicated below

Assembly location	Date code marking		
	Assy plant code	Assy year	Assy week
Morocco (ST)	CZ (on label) Z (on unit)	**Y** (1 digit indicating the year)	**WW** (2 digits indicating the week number)
China (subco)	**GP (on label)** **GP (on unit)**		

Traceability for the implemented change will be ensured by an **internal codification** and by the **Q.A. number**.

Qualification date	2020 week 08

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection device	TVS	SM15T100A	W14-2020
		SM15T100CA	W14-2020
		SM15T150CA	W14-2020
		SM15T200A	W14-2020
		SM15T200CA	W14-2020
		SM15T220A	W14-2020
		SM15T220CA	On request
		SMCJ85CA-TR	On request
		SMCJ130CA-TR	On request
		SMCJ170A-TR	On request
		SMCJ188A-TR	On request
		SMCJ188CA-TR	On request

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	2020 week 11	2020 week 22

Comments:	With early PCN acceptance, possible shipment starting week 14 on selected part numbers.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change.
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change.

Qualification results	20013QRP

Reliability Evaluation Report

SMCJxxA/CA from 85V to 188V (VRM)
SM15TxxA/CA from 100V to 220V(VBR)
Subcontractor in China

General Information	
Product Description	*1500W TVS in SMC*
Part Numbers	*SM15T100A/CA* *SM15T150A/CA* *SM15T200A/CA* *SM15T220A/CA* *SMCJ85A/CA* *SMCJ130A/CA* *SMCJ154A/CA* *SMCJ170A/CA* *SMCJ188A/CA*
Product Group	*ADG*
Product division	*DFD*
Package	*SMC*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*STMicroelectronics Tours (France)*
Assembly plant	*Subcontractor in China*
Reliability Lab	*STMicroelectronics Tours (France)*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	11/02/2019	8	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB / H3TRB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
RSH	Resistance to Solder Heat
SD	Solderability
DBT	Dead Bug Test
MSL	Moisture Sensitivity Level

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

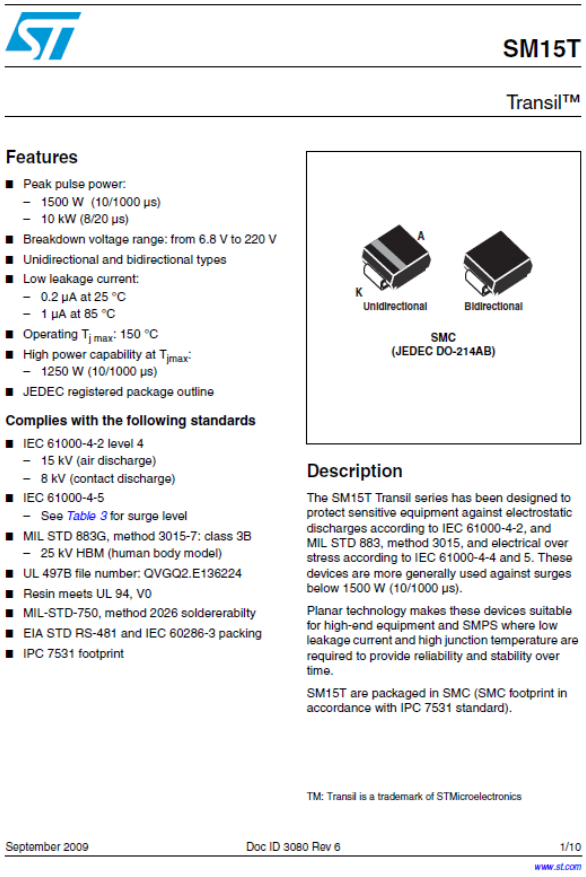
The aim of this report is to qualify 1500W unidirectional and bidirectional protection devices from 85V to 188V (VRM) housed in SMC package at our subcontractor in China.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description



SM15T

Transil™

Features

- Peak pulse power:
  - 1500 W (10/1000 µs)
  - 10 kW (8/20 µs)
- Breakdown voltage range: from 6.8 V to 220 V
- Unidirectional and bidirectional types
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating $T_{j\,max}$: 150 °C
- High power capability at T_{jmax}:
  - 1250 W (10/1000 µs)
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-5
  - See *Table 3* for surge level
- MIL STD 883G, method 3015-7: class 3B
  - 25 kV HBM (human body model)
- UL 497B file number: QVGQ2.E136224
- Resin meets UL 94, V0
- MIL-STD-750, method 2026 solderability
- EIA STD RS-481 and IEC 60286-3 packing
- IPC 7531 footprint

Description

The SM15T Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 1500 W (10/1000 µs).

Planar technology makes these devices suitable for high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

SM15T are packaged in SMC (SMC footprint in accordance with IPC 7531 standard).

TM: Transil is a trademark of STMicroelectronics

September 2009 Doc ID 3080 Rev 6 1/10

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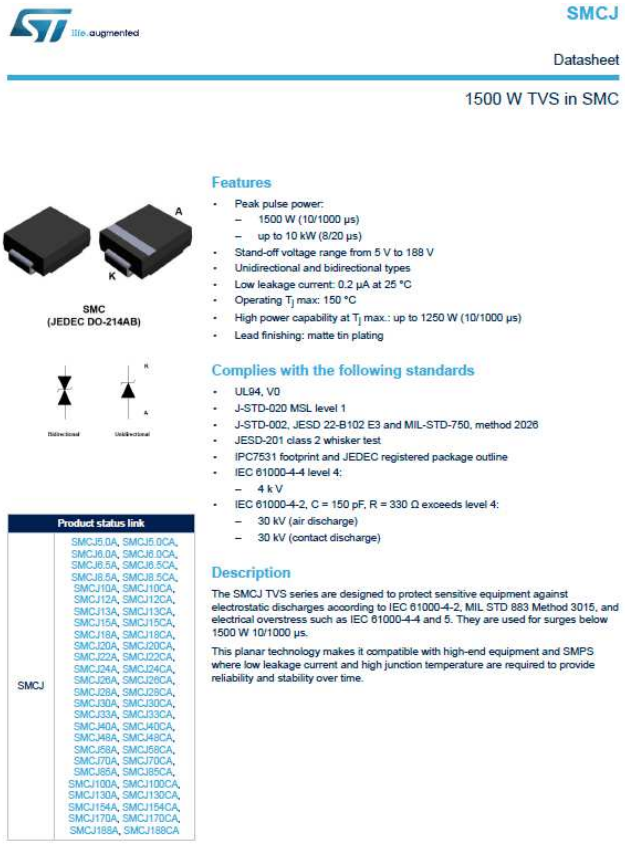

SMCJ

life.augmented

Datasheet

1500 W TVS in SMC

Features

- Peak pulse power:
  - 1500 W (10/1000 µs)
  - up to 10 kW (8/20 µs)
- Stand-off voltage range from 5 V to 188 V
- Unidirectional and bidirectional types
- Low leakage current: 0.2 µA at 25 °C
- Operating T_j max: 150 °C
- High power capability at T_j max.: up to 1250 W (10/1000 µs)
- Lead finishing: matte tin plating

Complies with the following standards

- UL94, V0
- J-STD-020 MSL level 1
- J-STD-002, JESD 22-B102 E3 and MIL-STD-750, method 2026
- JESD-201 class 2 whisker test
- IPC7531 footprint and JEDEC registered package outline
- IEC 61000-4-4 level 4:
  - 4 kV
- IEC 61000-4-2, C = 150 pF, R = 330 Ω exceeds level 4:
  - 30 kV (air discharge)
  - 30 kV (contact discharge)

Description

The SMCJ TVS series are designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, MIL STD 883 Method 3015, and electrical overstress such as IEC 61000-4-4 and 5. They are used for surges below 1500 W 10/1000 µs.

This planar technology makes it compatible with high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

Product status link	
SMCJ	SMCJ5.0A, SMCJ5.0CA, SMCJ6.0A, SMCJ6.0CA, SMCJ6.5A, SMCJ6.5CA, SMCJ8.5A, SMCJ8.5CA, SMCJ10A, SMCJ10CA, SMCJ12A, SMCJ12CA, SMCJ13A, SMCJ13CA, SMCJ15A, SMCJ15CA, SMCJ18A, SMCJ18CA, SMCJ20A, SMCJ20CA, SMCJ22A, SMCJ22CA, SMCJ24A, SMCJ24CA, SMCJ26A, SMCJ26CA, SMCJ28A, SMCJ28CA, SMCJ30A, SMCJ30CA, SMCJ33A, SMCJ33CA, SMCJ40A, SMCJ40CA, SMCJ48A, SMCJ48CA, SMCJ58A, SMCJ58CA, SMCJ70A, SMCJ70CA, SMCJ85A, SMCJ85CA, SMCJ100A, SMCJ100CA, SMCJ130A, SMCJ130CA, SMCJ154A, SMCJ154CA, SMCJ170A, SMCJ170CA, SMCJ188A, SMCJ188CA

4.2 Construction note

	SM15TxxA/CA (xx VRM from 100V to 220V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL FRANCE
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMC CLIP
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Commercial Product	Diffusion Plant	Assembly PLant	Package	Note
Lot 1	SM15T100CA	ST TOURS	SUBCONTRACTOR IN CHINA	SMC	Qualification lots
Lot 2	SM15T200A				
Lot 3	SM15T220CA				
Lot 4	SM30T56CAY				Same package for package oriented tests
Lot 5	SM30T56CAY				
Lot 6	SMD PACKAGE from subcontractor for whiskers assessment				

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.		
						Lot 1 VRM 85.5V	Lot 2 VRM 171V	Lot 3 VRM 188V
Die Oriented Tests								
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=150°C Tension=VRM	231	168h	0/77	0/77	0/77
					504h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77
Repetitive Surge	Y	ADCS0060282	IPP=11.5A/µs Pulse delay=0.01ms	20	50 surges	0/20	-	-
Repetitive Surge	Y	ADCS0060282	IPP=4.6A/µs Pulse delay=0.01ms	20	50 surges	-	-	0/20
Repetitive Surge	Y	ADCS0060282	IPP=5.5A/µs Pulse delay=0.01ms	20	50 surges	-	0/20	-
Package Oriented Tests								
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	77	500cy	-	0/77	-
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Tension=VRM or 100V if VRM>100V	231	504h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						Lot 4	Lot 5	Lot 6
Package oriented trials								
SD	N	JESD22 B-102	Steam Ageing SnAgCu bath 245°C	40	visual inspection	-	0/10	-
			Steam Ageing SnPb 220°C		visual inspection	-	0/10	-
			Dry Ageing SnAgCu 245°C		visual inspection	-	0/10	-
			Dry Ageing SnPb 220°C		visual inspection	-	0/10	-
DBT	N	DM 00112629	Fluxing followed by IR reflow.	30	Visual inspection	-	0/30	-
Whiskers	Y	AEC-Q005 JESD201	Pb free reflow TC -40°C/85°C 3 cycles/hrs	15	1500cy	-	-	0/15
			Pb free reflow THS 30°C/RH = 60%	15	4000hrs	-	-	0/15
			Pb free reflow THS 60°C / RH = 83%	15	4000hrs	-	-	0/15
			No reflow TC -55°C/85°C 10 min	15	1500cy	-	-	0/15
			No reflow THS 30°C / RH = 60%	15	4000hrs	-	-	0/15
			No reflow THS 55°C / RH = 85%	15	4000hrs	-	-	0/15
			SnPb reflow TC -55°C/85°C 10 min	15	1500cy	-	-	0/15
			SnPb reflow THS 30°C / RH = 60%	15	4000hrs	-	-	0/15
			SnPb reflow THS 55°C / RH = 85%	15	4000hrs	-	-	0/15
MSL Research	Y	JESD22 A-113	Humidity (HR)=85% MSL=1 Temperature=85°C	30	168h	0/30	-	-
RSH	Y	JESD22 A-111	Dippings=2 Temperature=260°C Time (off)=15s Time (on)=10s	30	168h	0/30	-	-

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Repetitive surges	ADCS0060282	Devices are submitted to rated Ipp for 1000 surges.	Purpose: This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.
Package Oriented			
uHAST	JESD22 A-118	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments .	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.
PC Preconditioning	JESD22 A-113	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

Test name	Standard Reference	Description	Purpose
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB/H3TRB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT Dead Bug Test	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.
Whiskers	AEC-Q005 JESD201	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).